Notice of Allowability	Application No.	Applicant(s)	
	09/668,408	ELLISON ET AL.	
	Examiner	Art Unit	
	Taghi T. Arani, Ph.D.	2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *6/21/2004*.

2. ☒ The allowed claim(s) is/are *2-6,8-15,17-24,26,27,29,30,47-51 and 53-75*.

3. ☐ The drawings filed on _____ are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 7/23/204
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

AYAZ SHEIKH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

DETAILED ACTION

Claims 1-60 were originally pending for examination.

Claims 1, 7, 16, 25, 28, 31-46, and 52 are cancelled by the amendment submitted 06/21/2004 and claims 61-75 are newly added.

Claims 2-6, 8-15, 17-24, 26-27, 29-30, 47-51, and 53-60 are amended.

Examiner's Statement of Reasons for Allowance

Claims 2-6,8-15, 17-24, 26-30, 47-51, 53-75 are allowed over prior art.

The following is an examiner's statement of reasons for the indication of allowable claimed subject matter.

As per claim 61 (the broader claim), prior art of record directed to Barnett et al. (US pate. No 6, 292,874) is directed to a system comprising:

a processor capable of selectively operating in a normal execution mode and,

alternatively, in an isolated execution mode [column 2, lines 47-65. i.e. a memory management unit provides two operating modes for the processing circuit. In a secure kernel mode and an application mode], the memory management unit translates the virtual memory address used by the software creator into physical address allocated to the application by the operating system in a secure kernel mode during installation];

a memory to include an isolated memory area accessible to the processor in the isolated execution mode [column 2, lines 47-65, i.e. the memory management unit of Barnett imposes firewalls between applications and permits hardware checked partitioning of the memory. The memory management unit provides two operating modes for the processing circuit. In a secure

kernel mode [i.e. isolated memory area], the programmer can access all resources of the device including hardware control];

Barnett fails to disclose a PE handler storage in the chipset circuit, the PE handler storage to store a PE handler image to be loaded into the isolated memory area after at least a portion of the chipset circuit is initialized.

Prior art of record directed to Carloganu et al. (US patent no. 6,226,749) is directed to method and apparatus for operating a set of resources under the control of a secure processor, e.g. security module (i.e. a chipset), having a command authentication means and a command execution means, to achieve secure control of the resources, see abstract.

The secure processor stores a set of command primitives for functional control of the resources. A set of defined commands for invoking command primitives has either a secured command format including a command sequence ID, a command code, and a set of command data items or a non-secured command format including a command code and a set of command data items.

The secure processor stores a command set up table including command type flags to designate each command as a secured command or a non-secured command. An application program running in an external device includes a plurality of the defined commands in either secured command format or the non-secured command format and these are sent one at a time to the secure processor for execution. The secure processor looks up each received command in the command set up table, and if the command is a non-secured command it immediately executes associated command primitives. If the command is a secured command, the secure processor

tests both its authenticity and regularity and only executes the associated command primitives if the command passes both tests.

US patent no. 6,226,749 fails to teach a PE handler storage in the chipset circuit, the PE handler storage to store a PE handler image to be loaded into the isolated memory area after at least a portion of the chipset circuit is initialized.

Prior art of record directed to Panwar relates to a method for dynamically reconfiguring a processor between uniprocessor and selected multiprocessor configurations (col. 2, lines 43-48).

Panwar teaches, in col. 13, lines 9-35, an instruction scheduling unit ISU 206 (see Fig. 8i.e. a chipset circuit) operative to schedule and dispatch instructions as soon as their dependencies have been satisfied into an appropriate execution unit (FGU 210). ISU 206 maintains trap status of live instructions and may perform other functions such as maintaining the correct architectural state of processor 102, including state maintenance when out-of-order instruction processing is used.

However, None of the prior arts of record, either taken by itself or in any combination, would have anticipated or made obvious the invention of the present application at or before the time it was filed. The subject matter regarded as allowable by the examiner is found in claims 61, 62,74 and 75, wherein a PE handler storage to store a "PE handler image" to be loaded into an "isolated memory area".

Dependent claims 2-6, 8-15, 17-24,26-27, 29-30, 47-51, 53-60, 63-73 are also allowed by virtue of their dependencies.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Taghi T. Arani whose telephone number is (703)305-4274. The examiner can normally be reached on 8:00-5:30 Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on (703) 305-9648. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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